Atty. Docket No. ACR0025-US (MTKI-04-218A)
Serial No: 09/828,202

Amendments to the Claims

Please amend the claims as follows:

1.   (Currently Amended) A system for decoding data, comprising:

a syndrome generator for generating a PI (Parity of Inner-code) direction syndrome and a PO (Parity of Outer-code) direction syndrome from an ECC (Error Correction Code) block comprising scrambled data, a PI, and a PO;

a memory that stores said PO direction syndrome during generation of said PO direction syndrome;

a data buffer for storing said ~~main~~scrambled data from said ECC block, said PI direction syndrome and said PO direction syndrome; and

an ECC decoder for performing error correction decoding of said scrambled data stored in said data buffer, using said PI direction syndrome and said PO direction syndrome.

2.   (Previously Presented) The system as claimed in claim 1 further comprising a data room to store said PI direction syndrome and said PO direction syndrome, wherein said ECC decoder accesses said PI direction syndrome and said PO direction syndrome from said data room for ensuing error correction decoding.

3.   (Currently Amended) The system as claimed in claim 2 wherein said syndrome generator reads said ECC block and transfers said ~~main~~scrambled data to said data buffer; and said ECC decoder reads said PI direction syndrome and said PO direction syndrome from said data buffer to said data room and repeats ECC decoding by accessing and correcting said PI direction syndrome and said PO direction syndrome in said data room and writing corrected ~~main~~scrambled data into said data buffer.

4.   (Previously Presented) The system as claimed in claim 1 further comprising a demodulator that receives and demodulates data from an optical disk to generate said ECC block and that converts M bit code words into N bit data symbols (M>N).

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5.   (Currently Amended) A method for decoding data, comprising the steps of:

(a) demodulating the data to generate an ECC (Error Correction Code) block that comprises ~~main~~scrambled data, a PI (Parity of Inner-code), and a PO (Parity of Outer-code);

(b) writing said ~~main~~scrambled data into a data buffer;

(c) calculating a PI direction syndrome from said PI and a PO direction syndrome from said PO, and storing PO direction syndrome data in a memory during calculating said PO direction syndrome;

(d) writing said PI direction syndrome and said PO direction syndrome into said data buffer;

(e) reading said PI and PO direction syndromes from said data buffer to an ECC decoder to perform error correction decoding of the PI and PO directions; and

(f) when errors are found, correcting said PI direction syndrome and said PO direction syndrome, and writing corrected scrambled main data into said data buffer.

6.   (Previously Presented) The method as claimed in claim 5 further comprising converting M bit code words into N bit data symbols (M>N).

7.   (Currently Amended) A system for decoding data, comprising:

a syndrome generator for generating a PI direction syndrome from an ECC (Error Correction Code) block that comprises scrambled data, a PI (Parity of Inner-code), and a PO (Parity of Outer-code);

a data buffer for storing said ~~main~~scrambled data, said PI direction syndrome and said PO; and

an ECC decoder for performing error correction decoding of said ~~main~~scrambled data, said PI direction syndrome and said PO.

8.   (Previously Presented) The system as claimed in claim 7 further comprising a memory that connects with said ECC decoder to store a PO direction syndrome calculated by said ECC decoder while performing PO direction error decoding.

9.   (Currently Amended) The system as claimed in claim 8 wherein said syndrome generator transfers said ~~mainscrambled~~ data, said PO and said PI direction syndrome to said data buffer; and said ECC decoder reads said ~~mainscrambled~~ data and said PO from said data buffer, ~~to~~ calculates said PO direction syndrome and performs error correction decoding of the PO direction, then writes said PO direction syndrome into said memory, corrects said PI direction syndrome and writes corrected ~~mainscrambled~~ data into said data buffer.

10.   (Previously Presented) The system as claimed in claim 7 further comprising a demodulator that receives and demodulates data from an optical disk to generate said ECC block and that converts M bit code words into N bit data symbols (M>N).

11.   (Currently Amended) A method for decoding data, comprising the steps of:
          (a) demodulating the data to generate an ECC (Error Correction Code) block that comprises main ~~scrambled~~ data, a PI (Parity of Inner-code), and a PO (Parity of Outer-code);
          (b) calculating a PI direction syndrome;
          (c) writing said PI direction syndrome, said main ~~scrambled~~ data and said PO into a data buffer;
          (d) reading said main ~~scrambled~~ data and said PO from said data buffer to an ECC decoder to calculate a PO direction syndrome and perform error correction decoding of the PO direction;
          (e) when errors are found, correcting said PO direction syndrome and said PI direction syndrome, and writing corrected main ~~scrambled~~ data into said data buffer;
          (f) reading said PI direction syndrome from said data buffer to said ECC decoder to perform error correction decoding of the PI direction; and
          (g) when errors are found, correcting said PO direction syndrome and said PI direction syndrome, and writing corrected main ~~scrambled~~ data into said data buffer.

12.   (Previously Presented) The method as claimed in claim 11 further comprising converting M bit code words into N bit data symbols (M>N).

13.   (Currently Amended) A decoding system for receiving and decoding data from an optical disk, comprising:

a demodulator for receiving and demodulating data from the disk to generate an ECC (Error Correction Code) block that comprises main data, a PI (Parity of Inner-code), and a PO (Parity of Outer-code);

a syndrome generator for generating a PI syndrome;

a data buffer for storing said main data, said PI syndrome and said PO;

a first de-scrambler and EDC (Error Detection Code) check for de-scrambling said main data stored in said data buffer and checking for errors in said main data;

an ECC decoder for performing error correction decoding of said ECC block;

a memory that connects with said ECC decoder to store a PO syndrome;

a second de-scrambler and EDC check for de-scrambling said main data and checking whether errors in said main data are corrected; and

an ATAPI (Advanced Technology Attachment Packet Interface) for reading said main data stored in said data buffer, then de-scrambling and transmitting said main data to a host.

14.   (Original) The decoding system as claimed in claim 13 wherein said syndrome generator reads said ECC block from said demodulator, then generates said PI syndrome and transfers said main data, said PO and said PI syndrome to said data buffer, meanwhile said main data is also transferred to said first de-scrambler and EDC check.

15.   (Previously Presented) The decoding system as claimed in claim 13 wherein said ECC decoder reads said PI syndrome from said data buffer to perform the error correction decoding of the PI direction, transfers a detected error to said second de-scrambler and EDC check to get the EDC check of the PI direction, corrects said PI syndrome and said PO in said data buffer, and writes corrected main data into said data buffer, afterward said ECC decoder reads said main data and said PO from said data buffer to generate said PO syndrome, writes said PO syndrome into said memory to perform error correction decoding of the PO direction,

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corrects said PO syndrome in said memory and said PI syndrome in said data buffer, and rewrites any further corrected main data into said data buffer.

16.   (Original) The decoding system as claimed in claim 13 wherein said demodulator converts M bit code words into N bit data symbols (M>N).

17.   (Previously Presented) A decoding method for receiving and decoding data from an optical disk, comprising the steps of:

(a) transmitting the data from the disk to a demodulator, wherein said demodulator demodulates the data to generate an ECC (Error Correction Code) block that comprises main data, a PI (Parity of Inner-code), and a PO (Parity of Outer-code);

(b) transmitting said ECC block to a syndrome generator to calculate a PI syndrome;

(c) writing said PI syndrome, said main data and said PO into a data buffer, and transmitting said main data to a first de-scrambler and EDC check to de-scramble said main data and check whether errors in said main data are corrected;

(d) reading said PI syndrome from said data buffer to an ECC decoder to perform error correction decoding of the PI direction, and transmitting any detected error to a second de-scrambler and EDC check to get the EDC check of the PI direction;

(e) correcting said PI syndrome and said PO in said data buffer and writing PI corrected main data into said data buffer;

(f) reading said main data and said PO from said data buffer to said ECC decoder to calculate a PO syndrome;

(g) writing said PO syndrome into a memory to perform error correction decoding of the PO direction;

(h) correcting said PO syndrome in said memory and correcting said PI syndrome in said data buffer, and writing PO corrected main data into said data buffer;

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(i) reading said main data from said data buffer to a second de-scrambler and
EDC check to de-scramble said main data and to check again whether errors in said main data
are corrected; and

(j) reading said main data from said data buffer to an ATAPI to de-scramble said
main data and transmit to the host.

18.   (Previously Presented) The decoding method as claimed in claim 17 wherein said
ECC block is generated by converting M bit code words into N bit data symbols (M>N).

19.   (Previously Presented) The decoding method as claimed in claim 17 wherein said
ECC decoder comprises a RSPC (Reed Solomon Product Code) structure.

20.   (Previously Presented) The decoding method as claimed in claim 17 wherein said
data buffer and said memory are independently selected from the group consisting of EDO-
RAM, SRAM, DRAM, SL-DRAM, DR-DRAM, EDO-DRAM, SDRAM, DDR-SDRAM, and
VC-SDRAM.

21.   (Currently Amended) The system as claimed in claim 1 wherein said data buffer
receives (i) said ~~mainscrambled~~ data and said PI direction syndrome from said syndrome
generator and (ii) said PO direction syndrome from said memory.

22.   (Currently Amended) The system as claimed in claim 1 further comprising a de-
scrambler and EDC (Error Detection Code) check for de-scrambling said ~~mainscrambled~~ data
stored in said data buffer and checking for errors in said ~~mainscrambled~~ data.

23.   (Currently Amended) The system as claimed in claim 1 further comprising an
ATAPI (Advanced Technology Attachment Packet Interface) for reading said ~~mainscrambled~~
data stored in said data buffer, then de-scrambling and transmitting said ~~mainscrambled~~ data to a
host.

24.   (Currently Amended) The method as claimed in claim 5 further comprising de-scrambling said ~~mainscrambled~~ data and checking for errors in said ~~mainscrambled~~ data.

25.   (Currently Amended) The method as claimed in claim 5 further comprising de-scrambling said ~~mainscrambled~~ data and transmitting said de-scrambled data to a host.

26.   (Previously Presented) The method as claimed in claim 5 further comprising abandoning said PI and said PO after said step of calculating said PI direction syndrome and said PO direction syndrome.

27.   (Previously Presented) The system as claimed in claim 7 further comprising a de-scrambler and EDC (Error Detection Code) check for de-scrambling said main data stored in said data buffer and checking for errors in said main data.

28.   (Previously Presented) The system as claimed in claim 7 further comprising an ATAPI (Advanced Technology Attachment Packet Interface) for reading said main data stored in said data buffer, de-scrambling and transmitting said main data to the host.

29.   (Currently Amended) The system as claimed in claim 7 wherein said ECC decoder reads said PI syndrome from said data buffer, performs error correction decoding of the PI direction, and when one or more errors are found, corrects said ~~mainscrambled~~ data and said PO in said data buffer.

30.   (Currently Amended) The system as claimed in claim 9 wherein said ECC decoder further reads said PI direction syndrome from said data buffer to perform ~~the~~ error correction of the PI direction, corrects said PI direction syndrome in said data buffer, corrects said PO direction syndrome in said data room, and writes the corrected ~~mainscrambled~~ data into said data buffer.

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31.   (Currently Amended) The method as claimed in claim 11 further comprising de-scrambling said mainscrambled data and checking for errors in said mainscrambled data.

32.   (Currently Amended) The method as claimed in claim 11 further comprising de-scrambling said mainscrambled data and transmitting said de-scrambled data to a host.

33.   (Previously Presented) The method as claimed in claim 11 further comprising abandoning said PI after said step of calculating said PI direction syndrome.